Cognitive radio platform: from achievable performance to architecture design

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Future mobile terminals will be able to communicate with various heterogeneous systems which are different by means of the algorithms used to implement baseband processing and channel coding. This represents many challenges in designing flexible and energy efficient architectures. The cognitive radio approach based on open air interface can build a very flexible framework able to cover different communications scenarios [1]. Using the sensing phase, the mobile can sense its environment and detect the spectrum holes and use them to communicate. The key feature of cognitive radios is their ability to recognize their communication environment and independently adapt the parameters of their communication scheme to maximize the quality of service (QoS) for the secondary (unlicensed) users while minimizing the interference to the primary users [2]. However, there are many challenges across all layers of a cognitive radio system design, from its application to its implementation.

In current research, we are investigating different techniques of using cognitive radio to reuse locally unused spectrum to increase the total system capacity. We consider a multiband/wideband system in which users wish to communicate to the base station, subject to mutual interference, and detect unused spectrum through adequate sensing. Current works aim also to develop efficient algorithm able to maximize the quality of service (QoS) for the secondary (unlicensed) users while minimizing the interference to the primary users. However, there are many challenges across all layers of a cognitive radio system design, from its application to its implementation.

Current research at Eurecom address the achievable performances of such systems with respect to classical communication systems (without cognition) [3] and highlight some practical cognitive protocols [4]. In particular, it is of major interest to show the fundamental principle of cognitive radios by proving, in which signal to noise ratio regime, such systems always perform better than classical ones. Moreover, moreover, we also determine the number of simultaneous users within a cognitive radio system. In fact, although cognitive radios have spurred great interest and excitement in industry, many of the fundamental theoretical questions on the limits of such technology remain unanswered.

On architecture design side, our platform is able to support different standards including: 3GPP, 802.11, WiMax (802.16), GSM, DVB etc as well as the reconfigurable *openairinterface.org* [5] radio interface. These standards although have common processing blocks like: Front End Processing,

Channel Coding / Decoding, Interleaving, Modulation / Demodulation etc. but each one has its own methodology and parameters. The proposed architecture has to cater these different methods and parameters in a reconfigurable manner in order to provide the seamless mobility to users.

The aimed reconfigurable architecture will take advantage of the commonalties that exist among the different schemes to be implemented but in an efficient manner. The commonalities and disjoints are translated into hardware architecture to come up with a system that performs all the required operation by all the applications.

The proposed hardware architecture is subdivided in two main parts: a high level control module and a Digital Signal Processing engine. They are implemented in high end Virtex-V FPGAs from Xilinx.

1) The control module is based on a Sparc CPU surrounded by its usual peripherals, external memories (SDRAM, Flash), a PCI-Cardbus interface and a dedicated interface with the DSP engine. The control module is in charge of controlling the DSP engine, implements some low-demanding processing (Phy and MAC) and interfaces the system with the host PC through the PCI-Cardbus interface. Most of the MAC layer processing runs on the host PC while the DSP engine executes most of the Phy layer processing tasks.

2) The DSP engine is a collection of data processing IP blocks plugged on a crossbar interconnect. Each IP block is a highly configurable and parameterizable processing unit dedicated to one class of algorithms (Fourier transforms, channel coding, channel decoding, modulation/demodulation, etc.) Some I/O blocks are also plugged on the interconnection to interface the DSP engine with its environment (the control module, the radio front end, the AD converters or some external resources). Some complex IP blocks are controlled by a local small micro-controller running a sequence of memory transfers and processing commands. Some others are controlled directly by the control module. The synchronization (inter or intra-blocks) is based on a set of interrupts signaling the end of memory transfers and of data processing. The control module programs the DSP engine by configuring the parameters and local software routines of the IP blocks.

Making a transceiver reconfigurable is generally limited by the radio-frequency (RF) and analog blocks as they do not lend themselves as easily to reconfiguration as the digital blocks. We present approaches to reconfigurable RF transceivers that are pursued in the research projects being carried out in Eurecom. The work can be divided into two parts. On the one hand, specific work on the architecture and building blocks for highly reconfigurable RF transceivers are developed. On the other hand, the concrete design and implementation of a prototype RF transceiver is presented. `

References:

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